DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT299

8-bit universal shift register; 3-state

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

8-bit universal shift register; 3-state 74HC/HCT299

FEATURES

- Multiplexed inputs/outputs provide improved bit density
- Four operating modes:
  - shift left
  - shift right
  - hold (store)
  - load data
- Operates with output enable or at high-impedance OFF-state (Z)
- 3-state outputs drive bus lines directly
- Can be cascaded for n-bits word length
- Output capability: bus driver (parallel I/Os), standard (serial outputs)
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT299 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT299 contain eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift-right, shift-left, parallel load and hold operations. The type of operation is determined by the mode select inputs (S_0 and S_1), as shown in the mode select table.
All flip-flop outputs have 3-state buffers to separate these outputs (I/O_0 to I/O_7) such, that they can serve as data inputs in the parallel load mode. The serial outputs (Q_0 and Q_7) are used for expansion in serial shifting of longer words.

A LOW signal on the asynchronous master reset input ($\overline{MR}$) overrides the S_n and clock (CP) inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock pulse. Inputs can change when the clock is either state, provided that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on the 3-state output enable inputs ($\overline{OE}_1$ or $\overline{OE}_2$) disables the 3-state buffers and the I/O_n outputs are set to the high-impedance OFF-state. In this condition, the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1, when in preparation for a parallel load operation.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	CP to Q_0, Q_7		20	19	ns
	CP to I/O_n		20	19	ns
t_{PHL}	$\overline{MR}$ to Q_0, Q_7 or I/O_n		20	23	ns
f_{max}	maximum clock frequency		50	46	MHz
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	120	125	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 19	S_0, S_1	mode select inputs
2, 3	$\overline{OE}_1$, $\overline{OE}_2$	3-state output enable inputs (active LOW)
7, 13, 6, 14, 5, 15, 4, 16	I/O_0 to I/O_7	parallel data inputs or 3-state parallel outputs (bus driver)
8, 17	Q_0, Q_7	serial outputs (standard output)
9	$\overline{MR}$	asynchronous master reset input (active LOW)
10	GND	ground (0 V)
11	D_{SR}	serial data shift-right input
12	CP	clock input (LOW-to-HIGH, edge-triggered)
18	D_{SL}	serial data shift-left input
20	V_{CC}	positive supply voltage

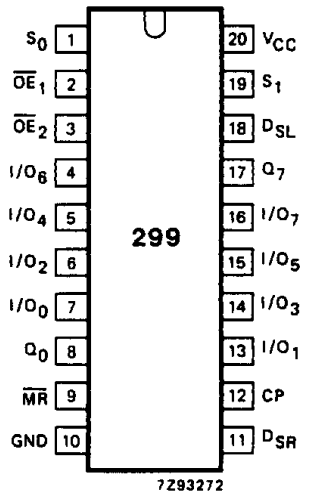


Fig.1 Pin configuration.

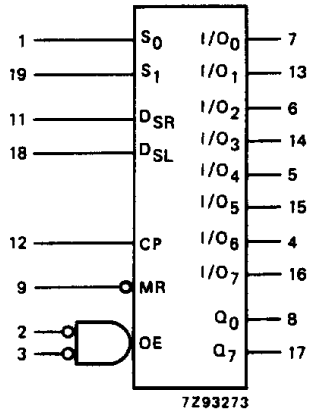


Fig.2 Logic symbol.

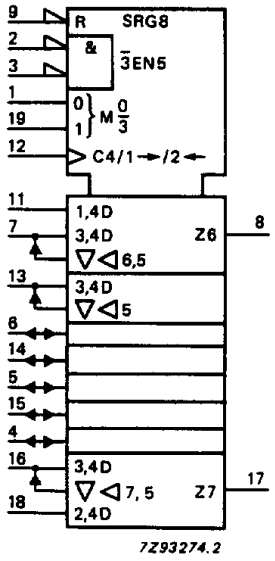


Fig.3 IEC logic symbol.

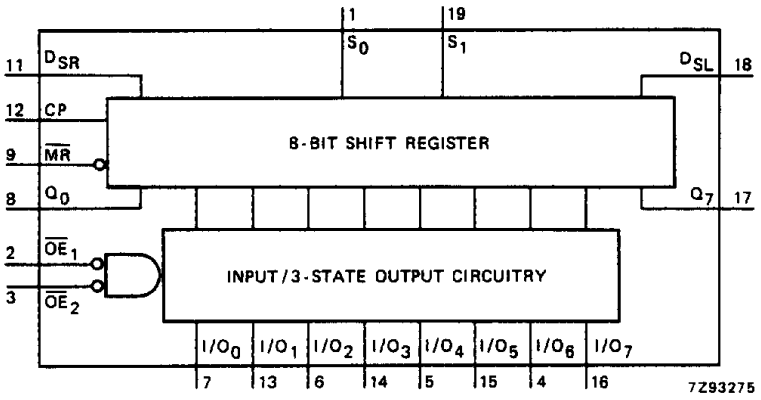


Fig.4 Functional diagram.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	asynchronous reset; Q_0–Q_7 = LOW
H	H	H	↑	parallel load; $I/O_n \rightarrow Q_n$
H	L	H	↑	shift right; $D_{SR} \rightarrow Q_0$, $Q_0 \rightarrow Q_1$ etc.
H	H	L	↑	shift left; $D_{SL} \rightarrow Q_7$, $Q_7 \rightarrow Q_6$ etc.
H	L	L	X	hold

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH CP transition

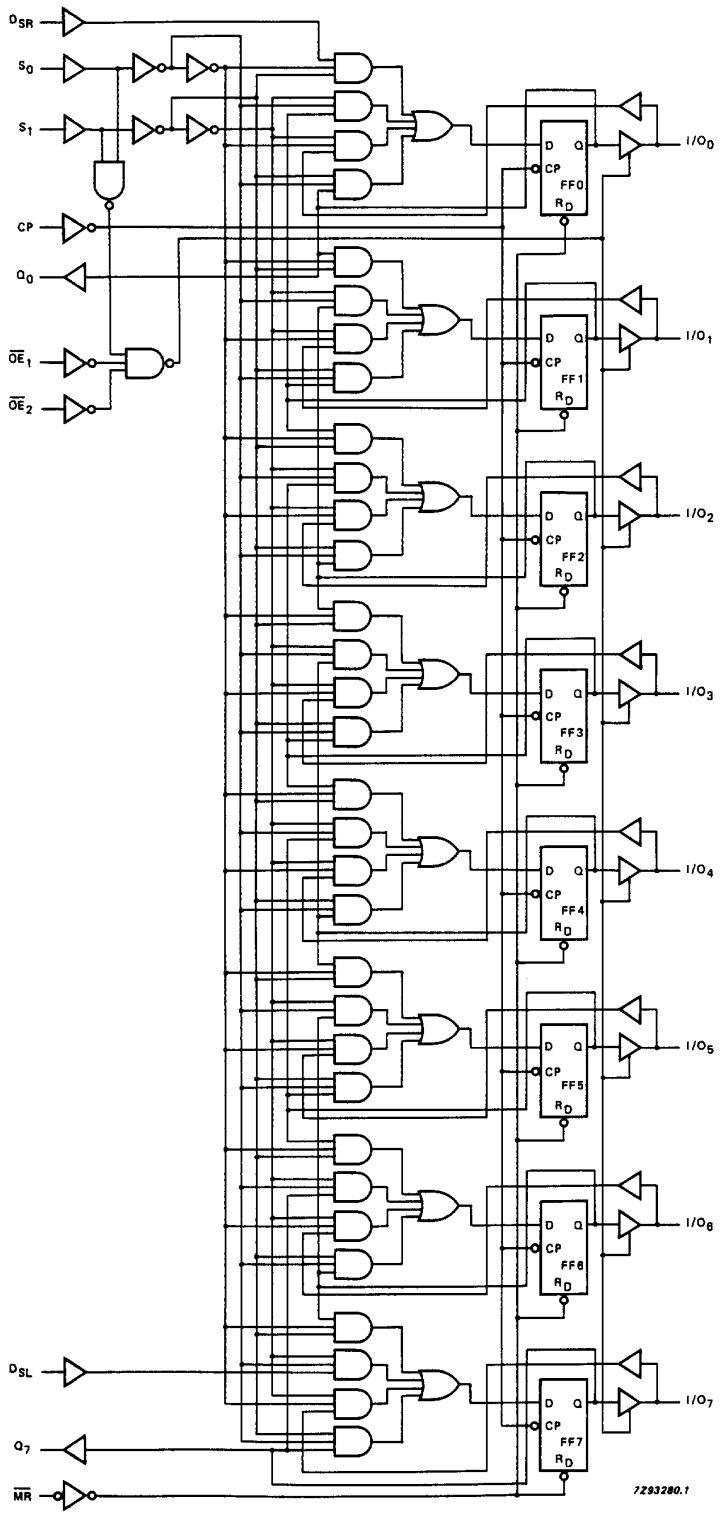


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver (parallel I/Os)
standard (serial outputs)
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_0, Q_7		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay CP to I/O_n		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/	propagation delay $\overline{MR}$ to Q_0, Q_7 or I/O_n		66 24 19	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.7
t_{PZH}	3-state output enable time $\overline{OE}_n$ to I/O_n		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.9
t_{PZL}	3-state output enable time $\overline{OE}_n$ to I/O_n		41 15 12	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig.9
t_{PHZ}	3-state output disable time $\overline{OE}_n$ to I/O_n		66 24 19	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig.9
t_{PLZ}	3-state output disable time $\overline{OE}_n$ to I/O_n		55 20 16	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.9
t_{THL}/ t_{TLH}	output transition time bus driver (I/O_n)		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t_{THL}/ t_{TLH}	output transition time standard (Q_0, Q_7)		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_W	master reset pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{rem}	removal time $\overline{MR}$ to CP	5 5 5	−14 −5 −4		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time D_{SR}, D_{SL} to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.6
t_{su}	set-up time S_0, S_1 to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.8
t_{su}	set-up time I/O_n to CP	125 25 21	39 14 11		155 31 26		190 38 32		ns	2.0 4.5 6.0	Fig.6
t_h	hold time I/O_n, D_{SR}, D_{SL} to CP	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.6
t_h	hold time S_0, S_1 to CP	0 0 0	−28 −10 −8		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.8
f_{max}	maximum clock pulse frequency	5.0 25 29	15 45 54		4.0 20 24		3.4 17 20		MHz	2.0 4.5 6.0	Fig.6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver (parallel I/Os)
standard (serial outputs)
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

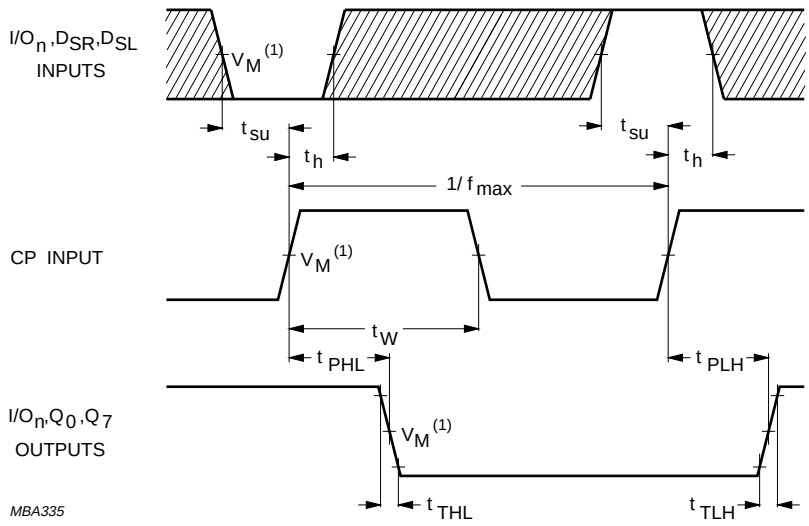
INPUT	UNIT LOAD COEFFICIENT
I/O_n	0.25
D_{SR}, D_{SL}	0.25
$\overline{CP}$, S_0	0.60
$\overline{MR}$, S_1	0.25
$\overline{OE}_n$	0.30

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_0, Q_7		22	37		46		56	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay CP to I/O_n		22	37		46		56	ns	4.5	Fig.6
t_{PHL}	propagation delay $\overline{MR}$ to Q_0, Q_7 or I/O_n		27	46		58		69	ns	4.5	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to I/O_n		19	30		38		45	ns	4.5	Fig.9
t_{PHZ}	3-state output disable time $\overline{OE}_n$ to I/O_n		24	37		46		56	ns	4.5	Fig.9
t_{PLZ}	3-state output disable time $\overline{OE}_n$ to I/O_n		20	32		40		48	ns	4.5	Fig.9
t_{THL}/ t_{TLH}	output transition time bus driver (I/O_n)		5	12		15		18	ns	4.5	Fig.6
t_{THL}/ t_{TLH}	output transition time standard (Q_0, Q_7)		7	15		19		22	ns	4.5	Fig.6
t_W	clock pulse width HIGH or LOW	20	10		25		30		ns	4.5	Fig.6
t_W	master reset pulse width LOW	20	11		25		30		ns	4.5	Fig.7
t_{rem}	removal time $\overline{MR}$ to CP	10	2		9		11		ns	4.5	Fig.7
t_{su}	set-up time I/O_n, D_{SR}, D_{SL} to CP	25	14		31		38		ns	4.5	Fig.6
t_{su}	set-up time S_0, S_1 to CP	32	18		40		48		ns	4.5	Fig.8
t_h	hold time I/O_n, D_{SR}, D_{SL} to CP	0	−11		0		0		ns	4.5	Fig.6
t_h	hold time S_0, S_1 to CP	0	−17		0		0		ns	4.5	Fig.8
f_{max}	maximum clock pulse frequency	25	42		20		17		MHz	4.5	Fig.6

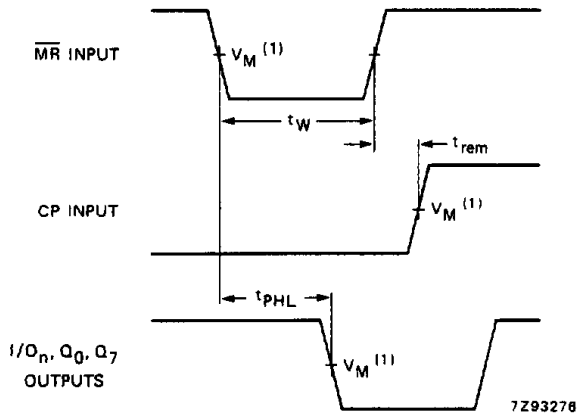
AC WAVEFORMS



The shaded areas indicate when the input is permitted to change for predictable output performance.

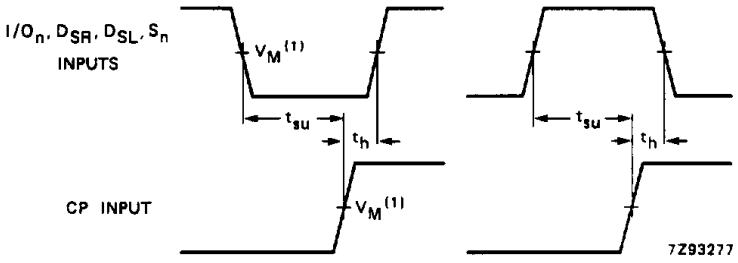
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the clock (CP) to output (I/O_n, Q_0, Q_7) propagation delays, the clock pulse width, the I/O_n, D_{SR} and D_{SL} to CP set-up and hold times, the output transition times and the maximum clock frequency.



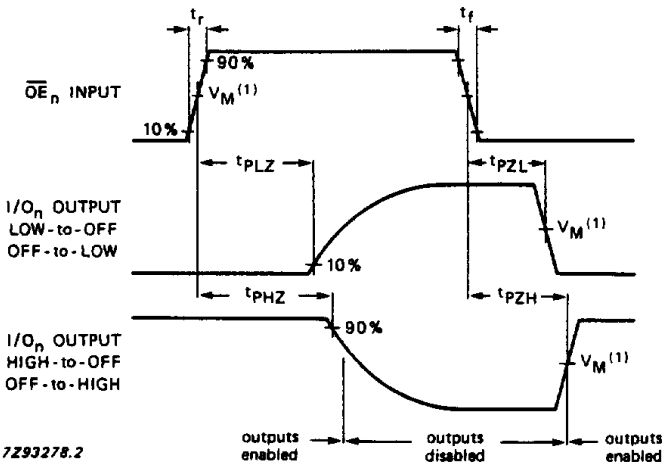
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the master reset ($\overline{MR}$) pulse width (LOW), the master reset to output (I/O_n, Q_0, Q_7) propagation delays and the master reset to clock (CP) removal time.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the set-up and hold times from the mode control inputs (S_0, S_1) to the clock (CP).



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the 3-state enable and disable times for $\overline{OE}_n$ inputs.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.